Figure 1

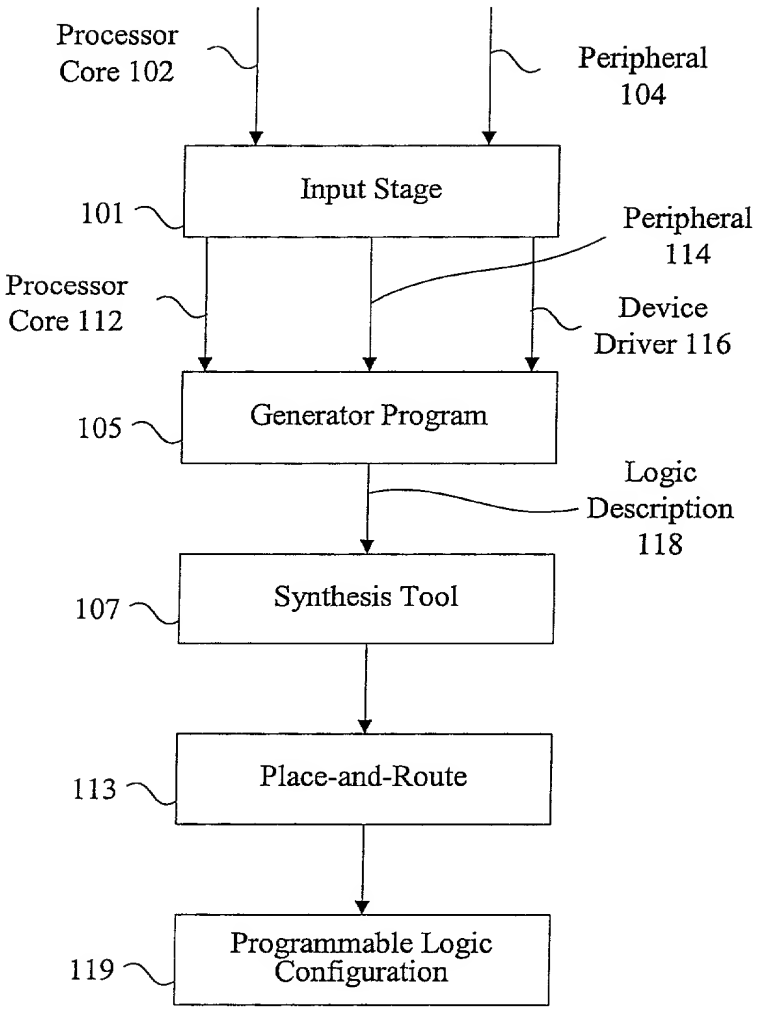

Processor Core 102
Peripheral 104
Input Stage
101
Peripheral 114
Processor Core 112
Device Driver 116
Generator Program
105
Logic Description 118
Synthesis Tool
107
Place-and-Route
113
Programmable Logic Configuration
119

Figure 2

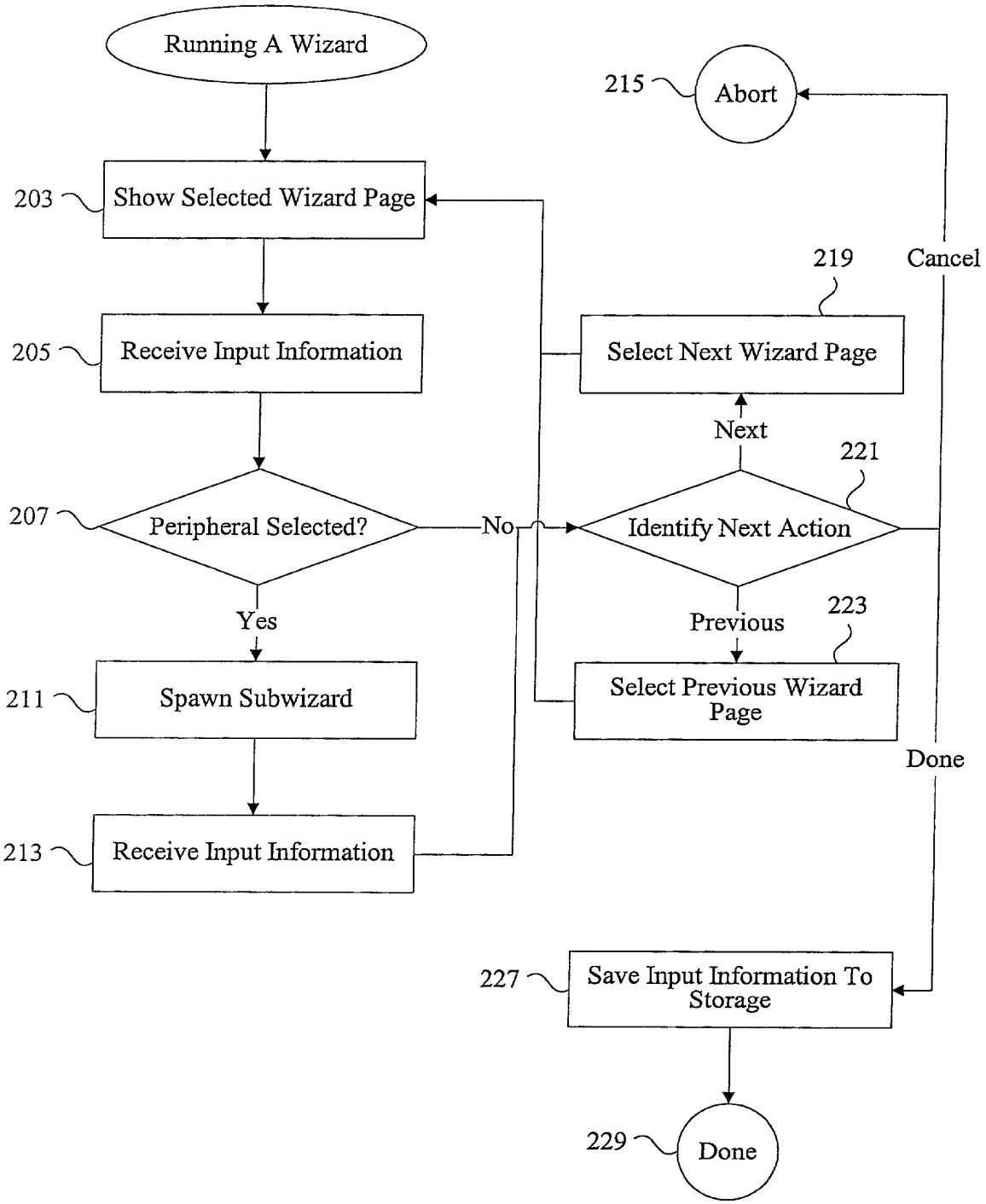

Running A Wizard
215
Abort
203
Show Selected Wizard Page
219
Cancel
205
Receive Input Information
Select Next Wizard Page
Next
221
207
Peripheral Selected?
No
Identify Next Action
Yes
Previous
223
211
Spawn Subwizard
Select Previous Wizard Page
Done
213
Receive Input Information
227
Save Input Information To Storage
229
Done

FIGURE 3A

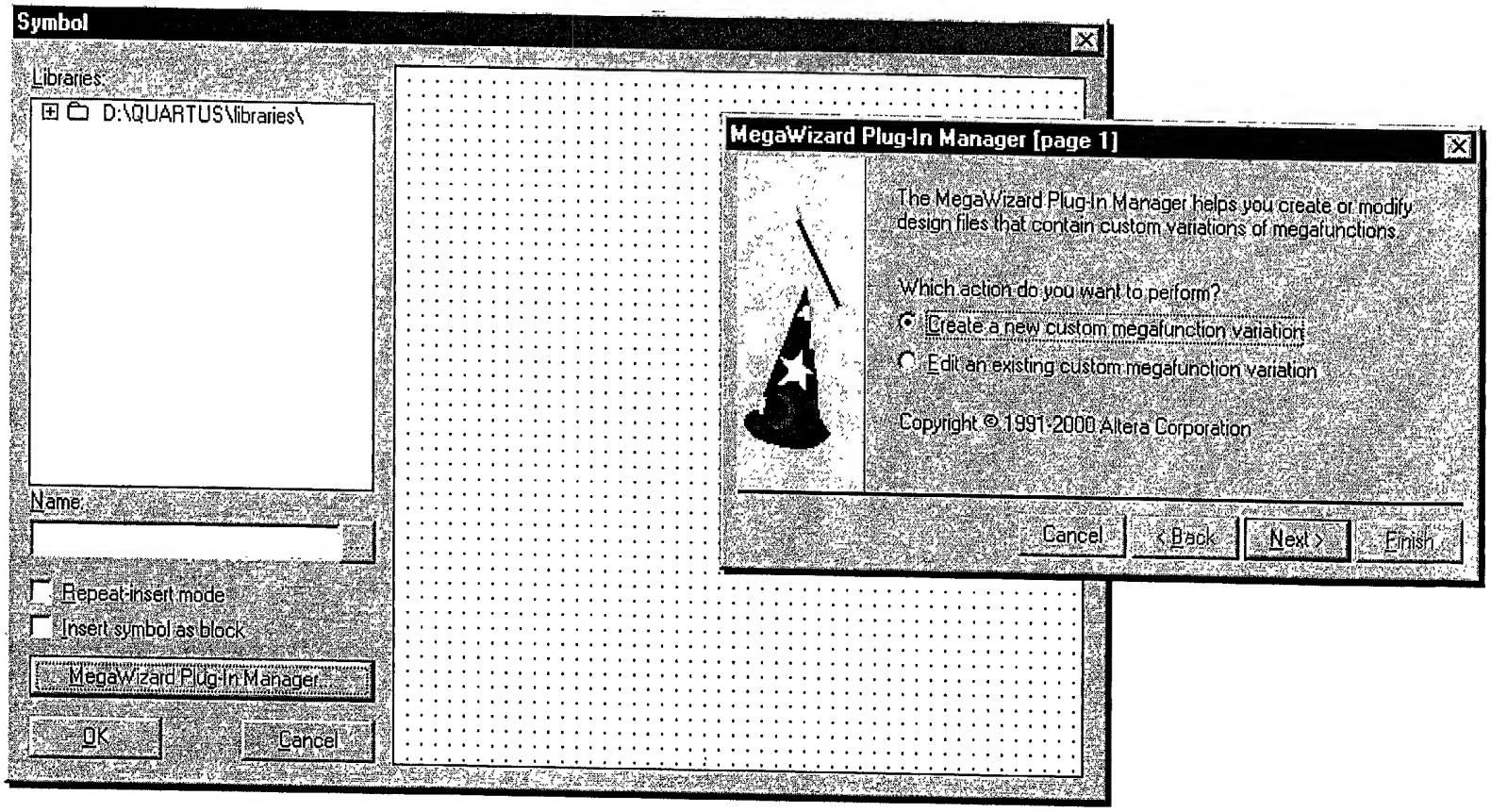

Symbol
Libraries:
D:\QUARTUS\libraries\
Name:
Repeat-insert mode
Insert symbol as block
MegaWizard Plug-In Manager...
OK
Cancel
MegaWizard Plug-In Manager [page 1]
The MegaWizard Plug-In Manager helps you create or modify design files that contain custom variations of megafunctions.
Which action do you want to perform?
Create a new custom megafunction variation
Edit an existing custom megafunction variation
Copyright © 1991-2000 Altera Corporation
Cancel
< Back
Next >
Finish

FIGURE 3B

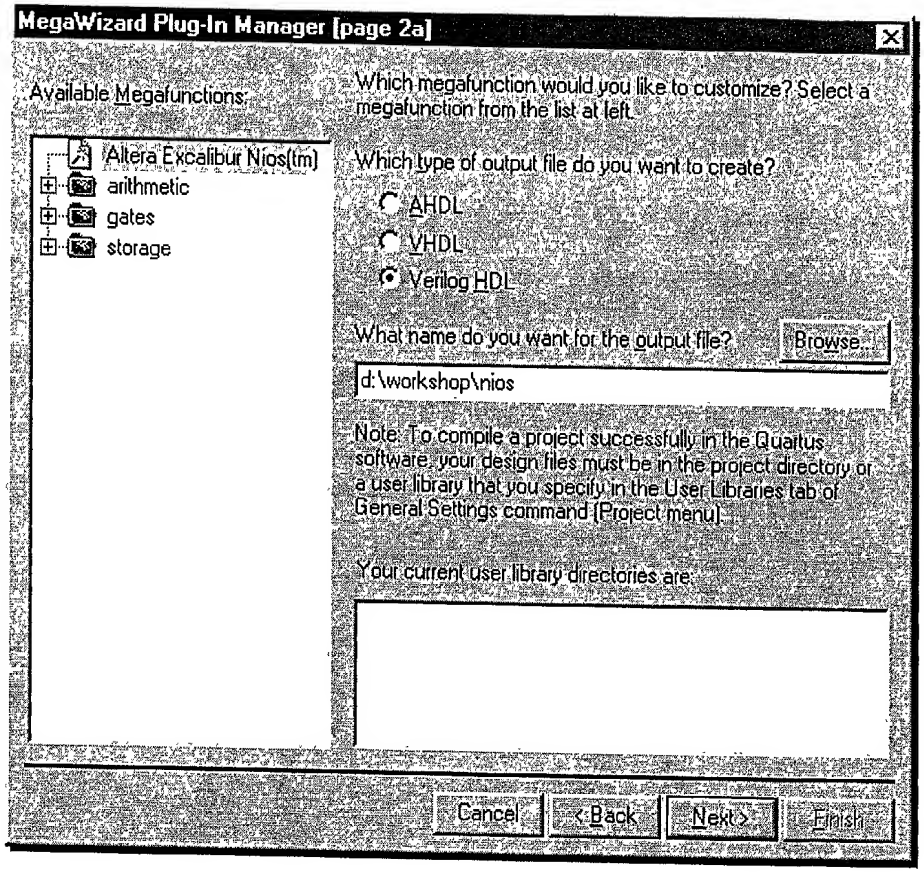


FIGURE 3C

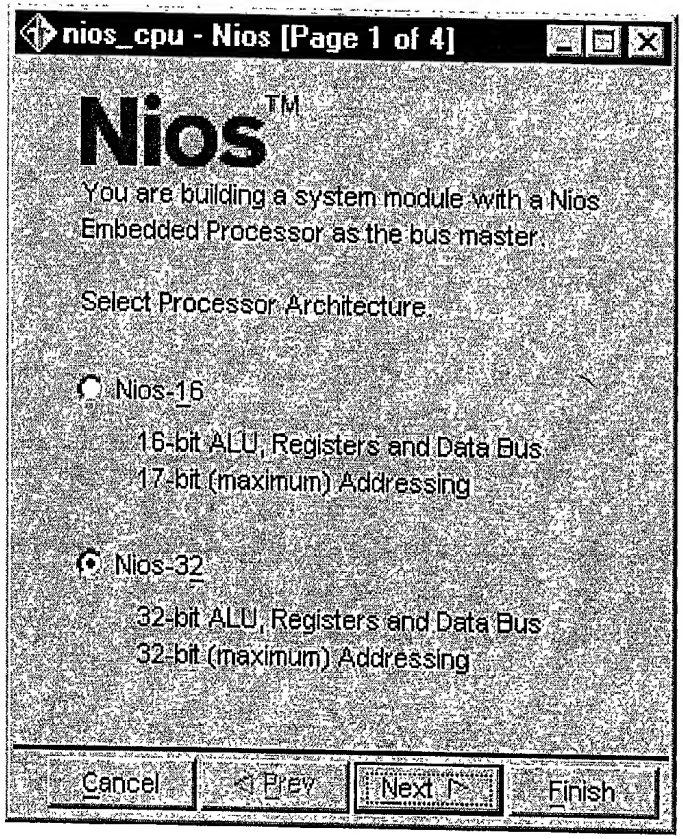

nios_cpu - Nios [Page 1 of 4]
Nios™
You are building a system module with a Nios Embedded Processor as the bus master.
Select Processor Architecture
Nios-16
16-bit ALU, Registers and Data Bus
17-bit (maximum) Addressing
Nios-32
32-bit ALU, Registers and Data Bus
32-bit (maximum) Addressing
Cancel
< Prev
Next >
Finish

FIGURE 3D

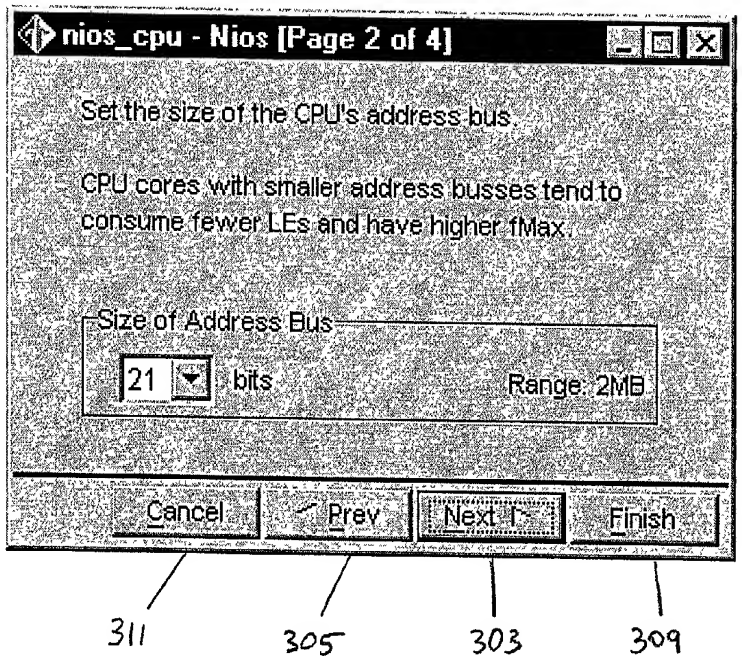


FIGURE 3E

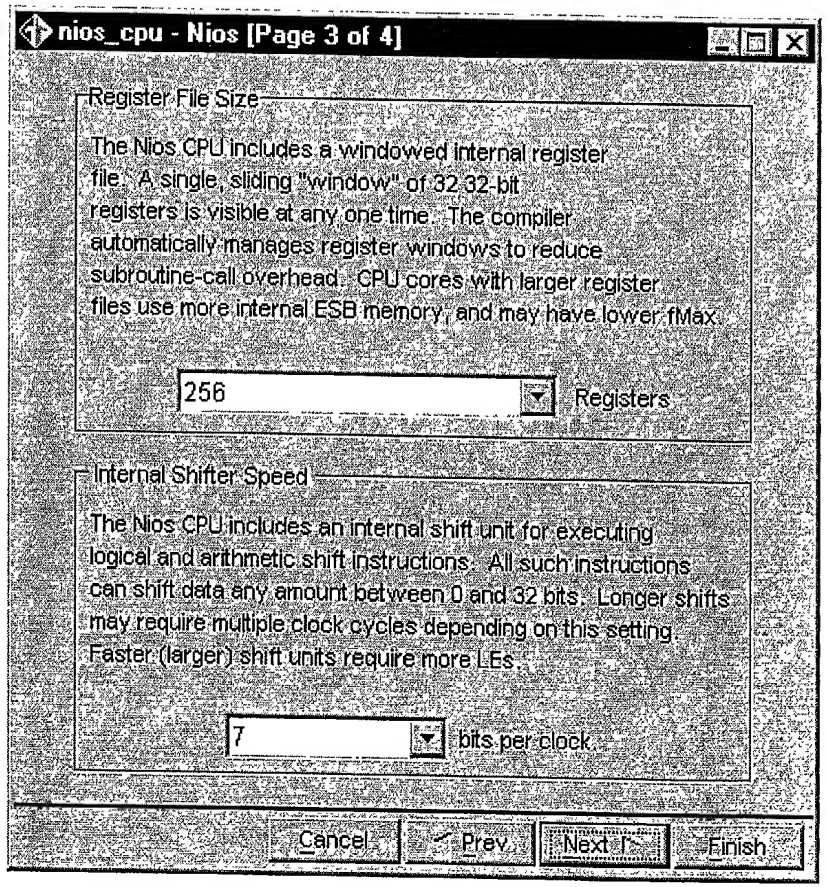


FIGURE 3F

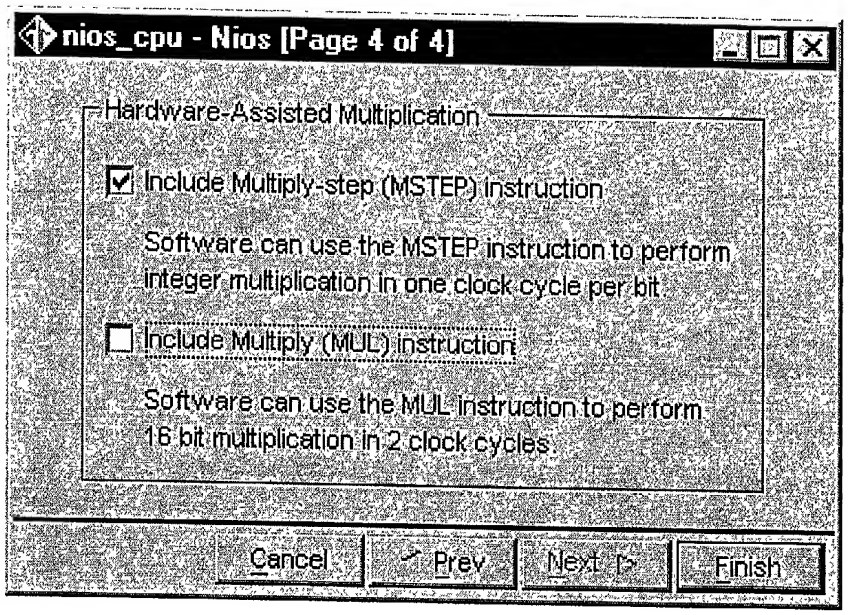


FIGURE 3G

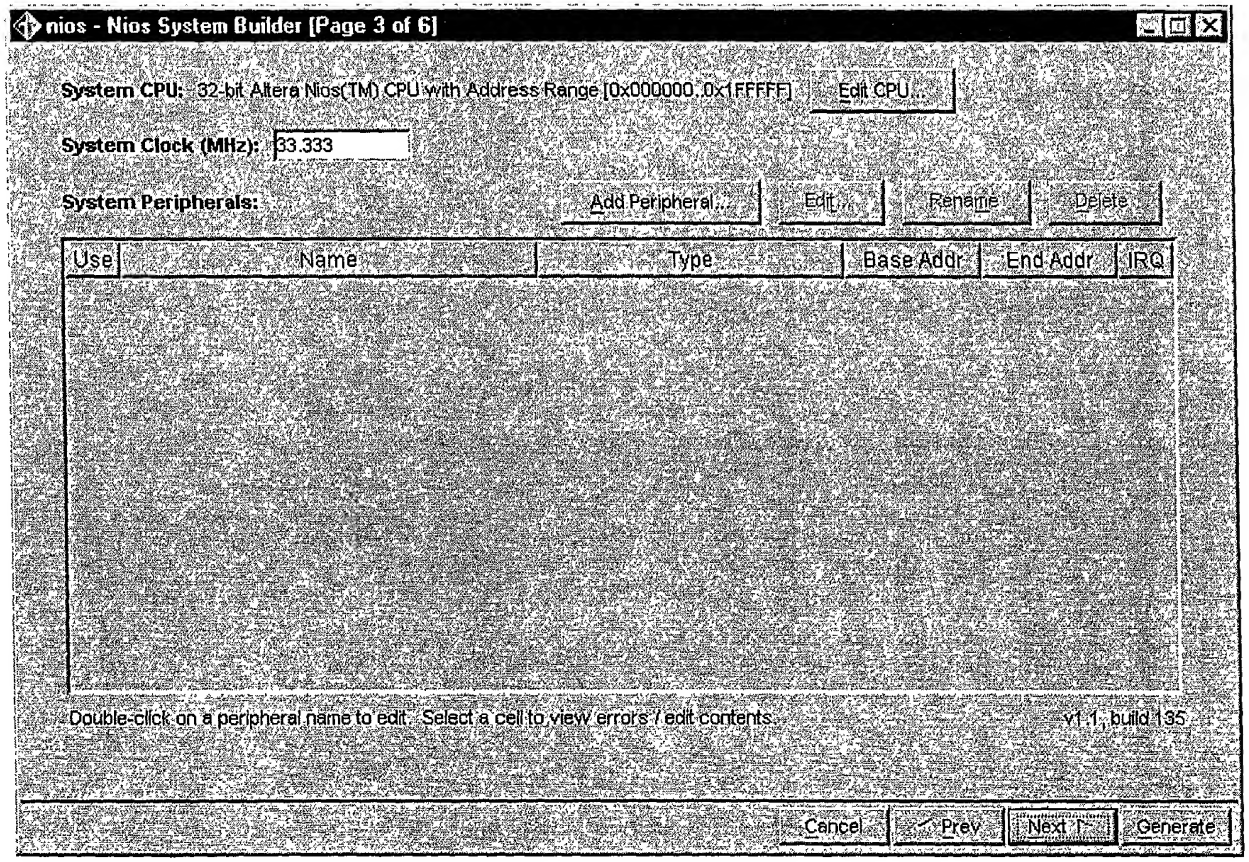


FIGURE 3H

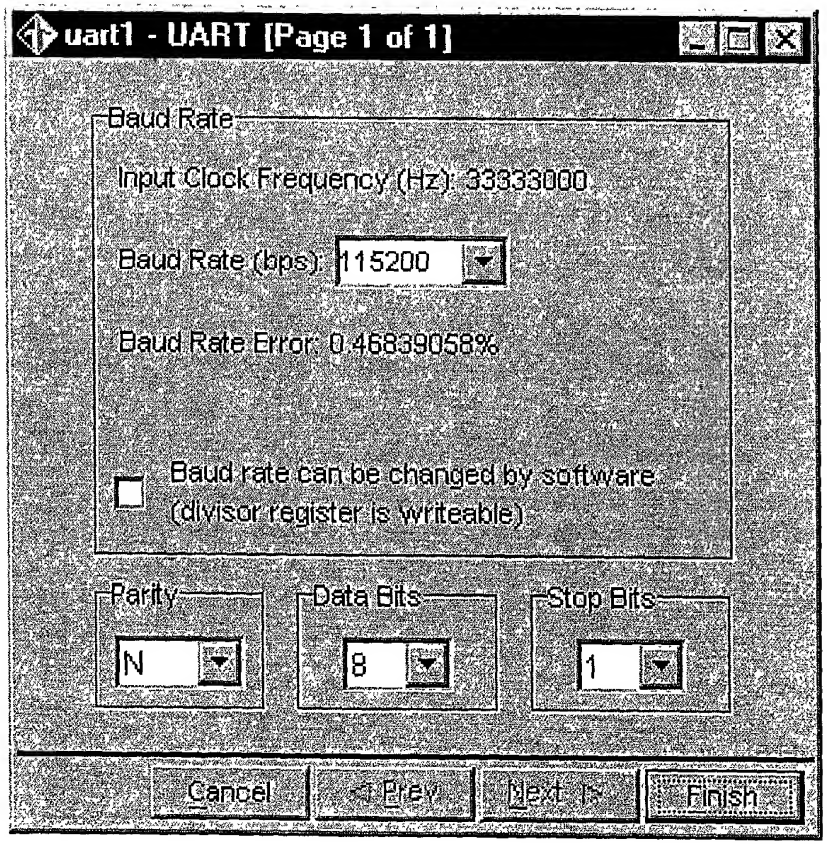


FIGURE 3I

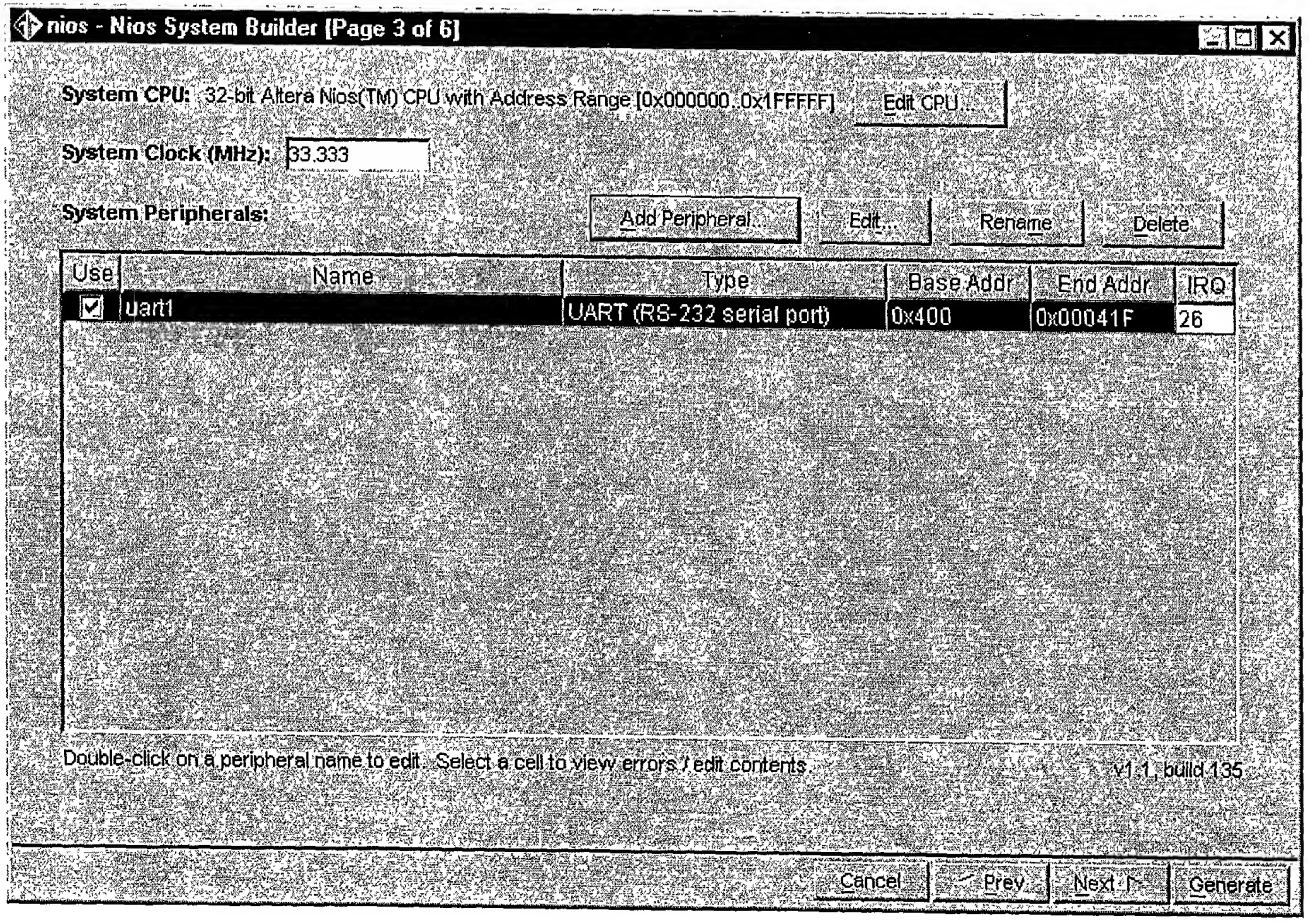


FIGURE 3J

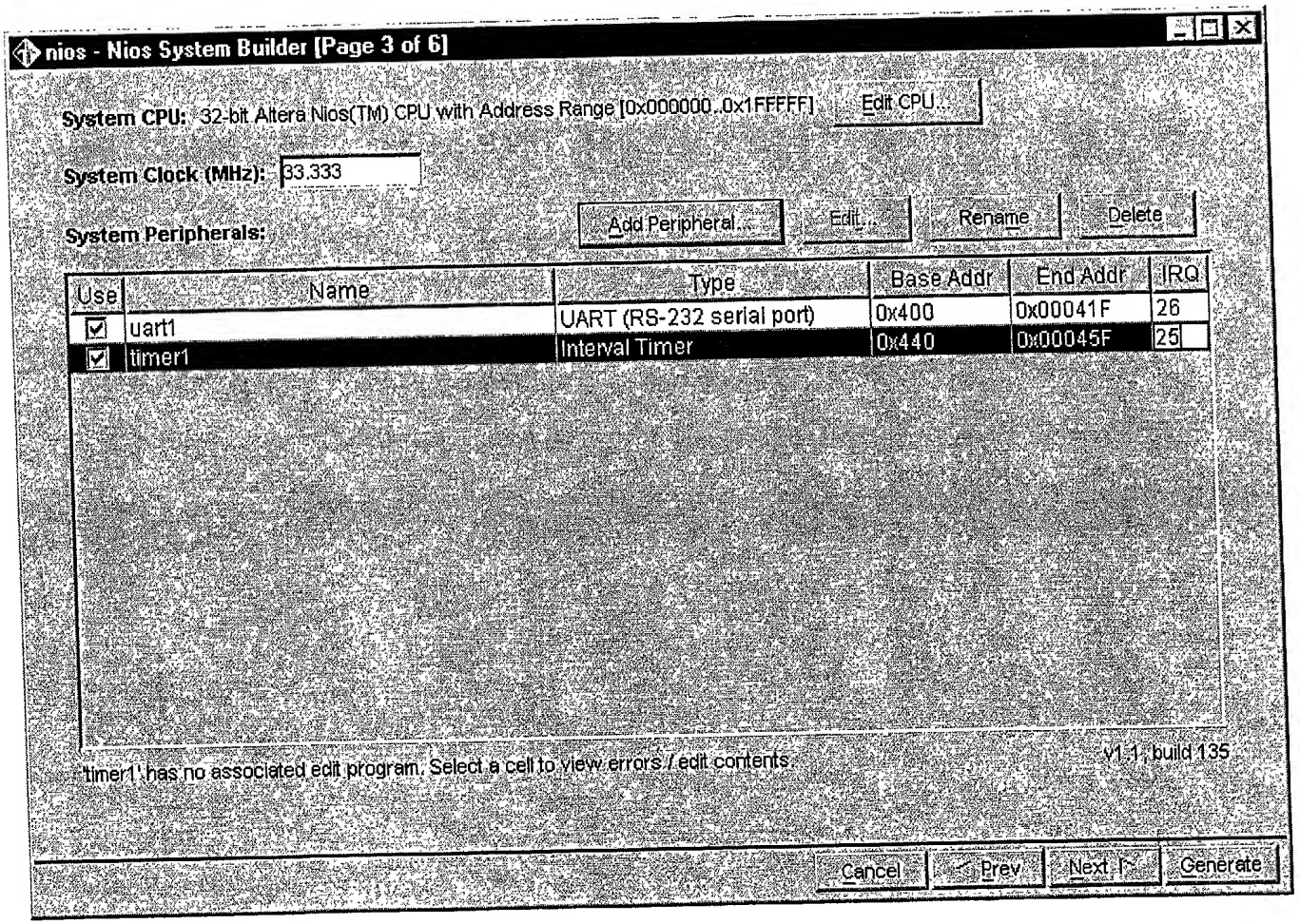

nios - Nios System Builder [Page 3 of 6]
System CPU: 32-bit Altera Nios(TM) CPU with Address Range [0x000000..0x1FFFFF]
Edit CPU...
System Clock (MHz): 33.333
System Peripherals:
Add Peripheral...
Edit...
Rename
Delete
Use
Name
Type
Base Addr
End Addr
IRQ
uart1
UART (RS-232 serial port)
0x400
0x00041F
26
timer1
Interval Timer
0x440
0x00045F
25
'timer1' has no associated edit program. Select a cell to view errors / edit contents.
v1.1 build 135
Cancel
< Prev
Next >
Generate

FIGURE 3K

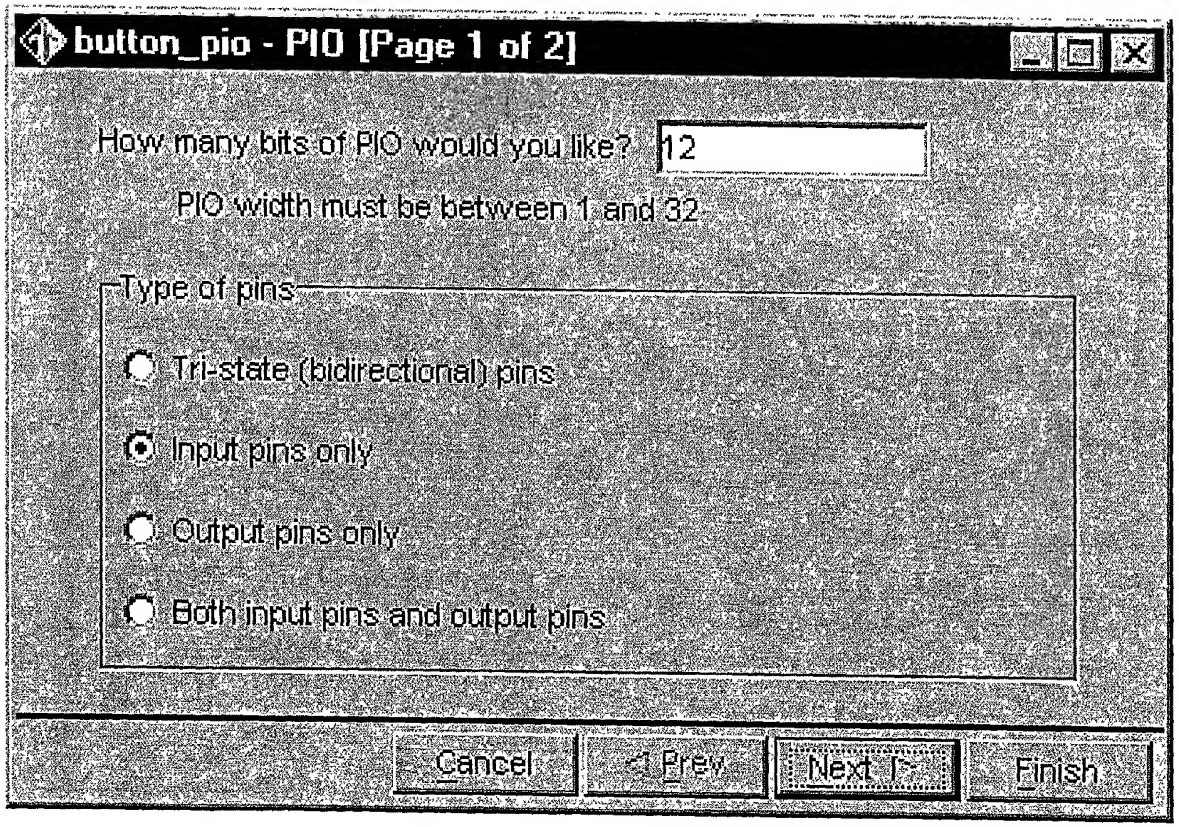


FIGURE 3L

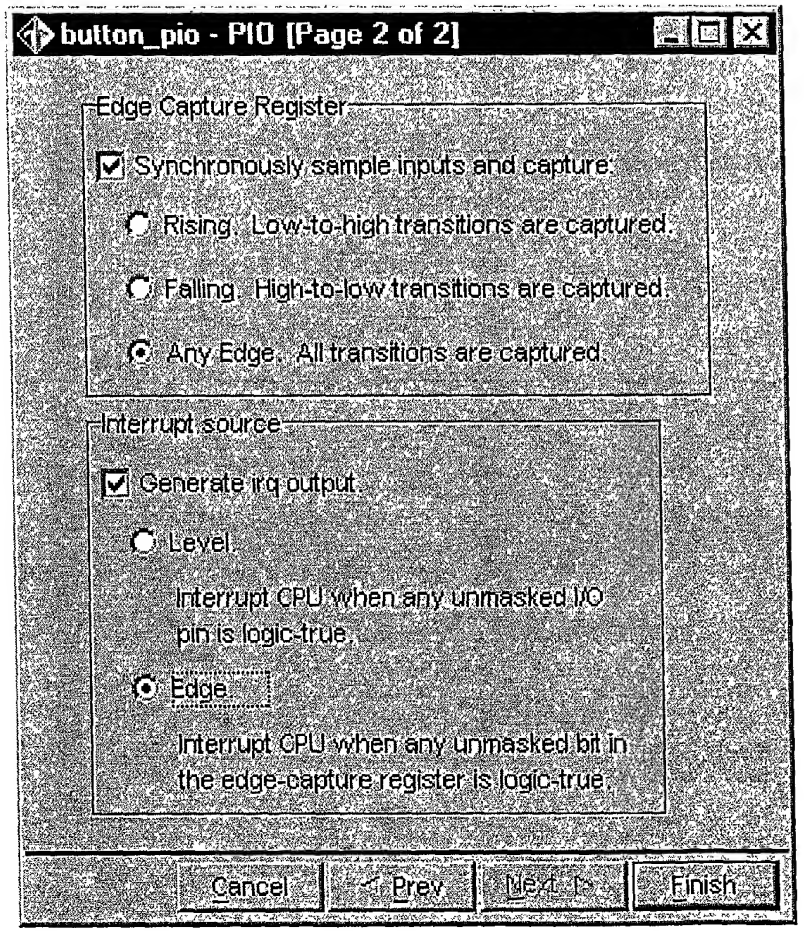


FIGURE 3M

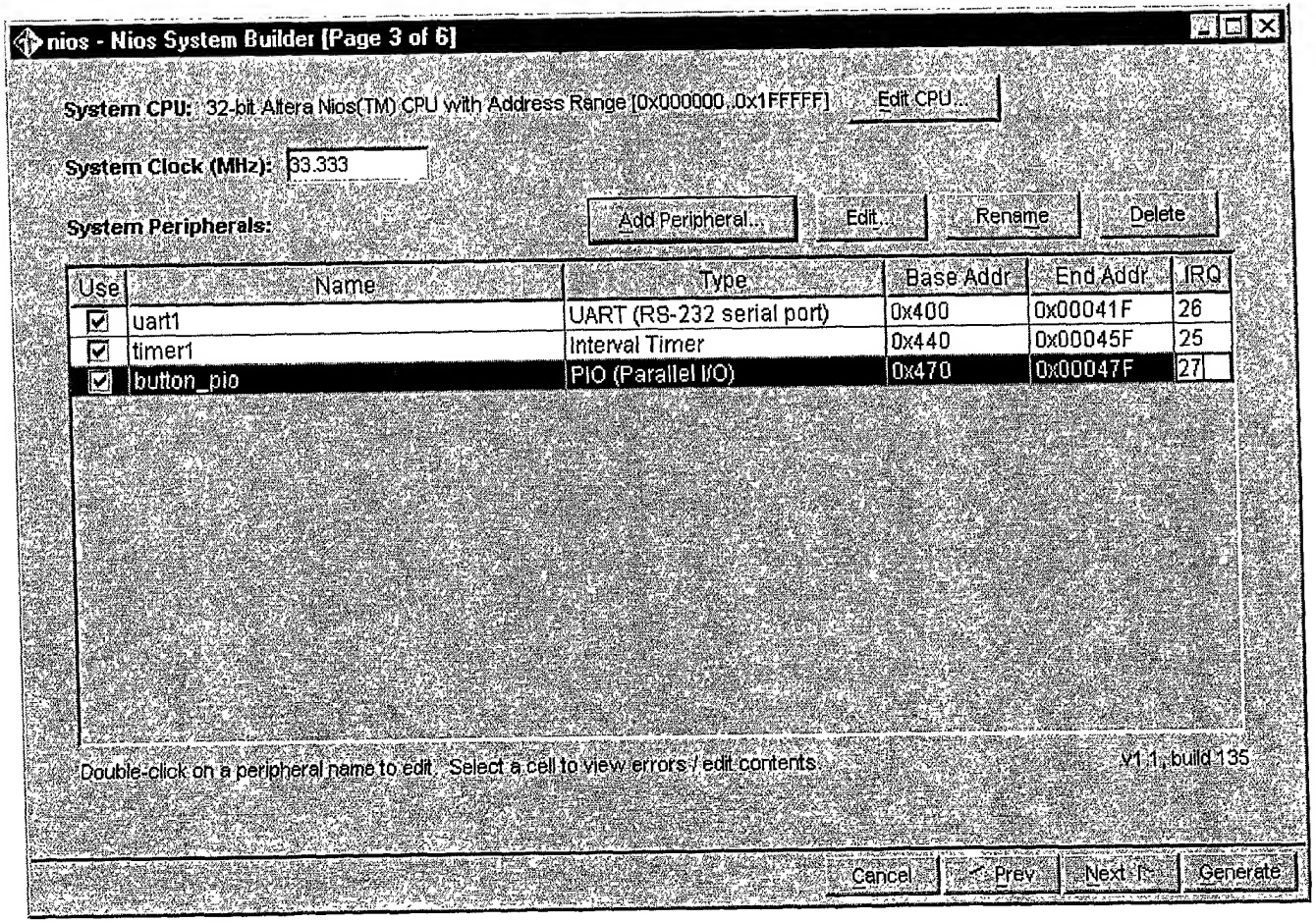
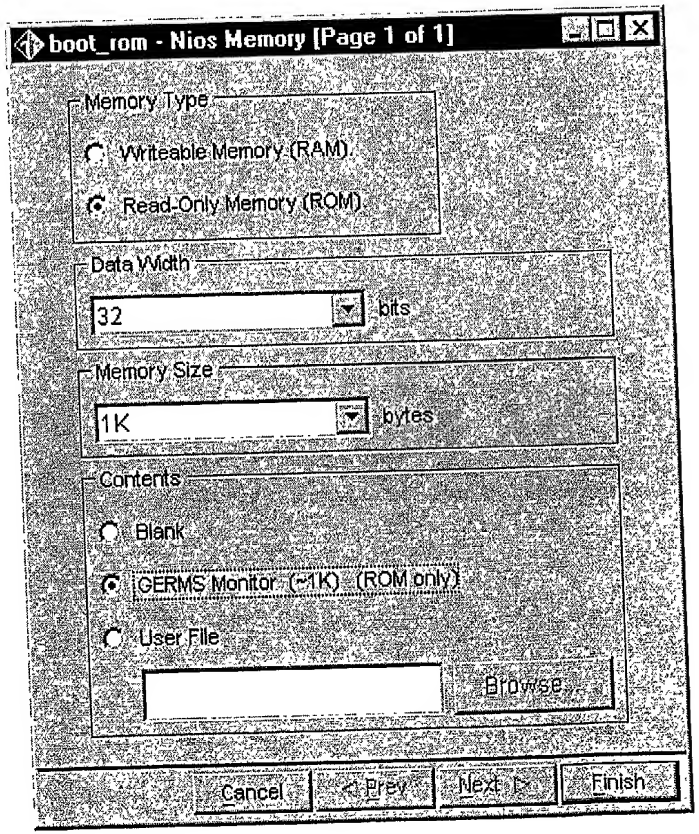

nios - Nios System Builder [Page 3 of 6]
System CPU: 32-bit Altera Nios(TM) CPU with Address Range [0x000000..0x1FFFFF]
Edit CPU...
System Clock (MHz): 33.333
System Peripherals:
Add Peripheral...
Edit...
Rename
Delete
Use
Name
Type
Base Addr
End Addr
IRQ
uart1
UART (RS-232 serial port)
0x400
0x00041F
26
timer1
Interval Timer
0x440
0x00045F
25
button_pio
PIO (Parallel I/O)
0x470
0x00047F
27
Double-click on a peripheral name to edit. Select a cell to view errors / edit contents.
v1.1 build 135
Cancel
< Prev
Next >
Generate

FIGURE 3N


boot_rom - Nios Memory [Page 1 of 1]
Memory Type
Writeable Memory (RAM)
Read-Only Memory (ROM)
Data Width
32
bits
Memory Size
1K
bytes
Contents
Blank
GERMS Monitor (~1K) (ROM only)
User File
Browse...
Cancel
< Prev
Next >
Finish

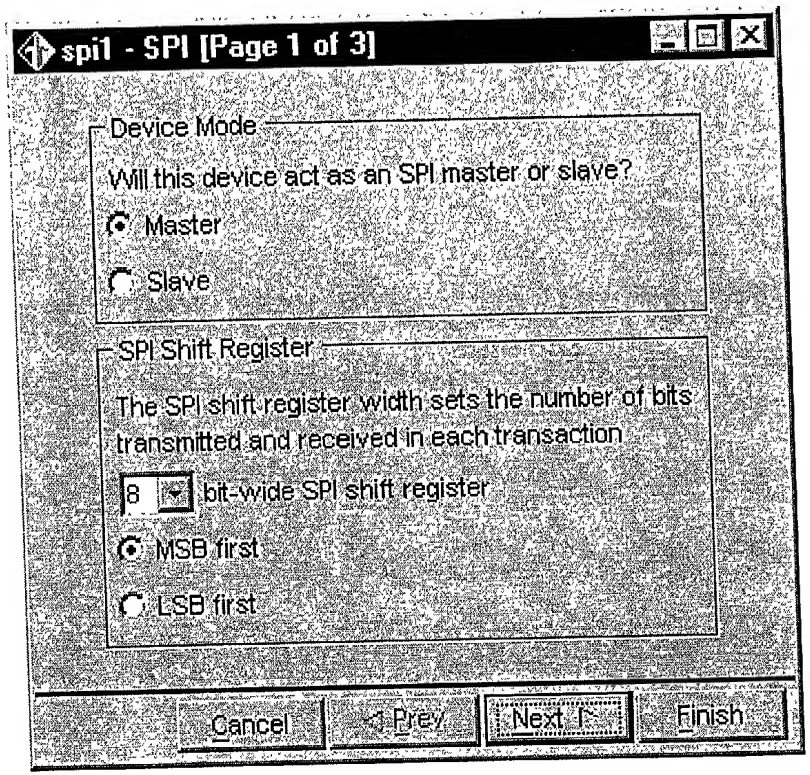


FIGURE 30

FIGURE 3P

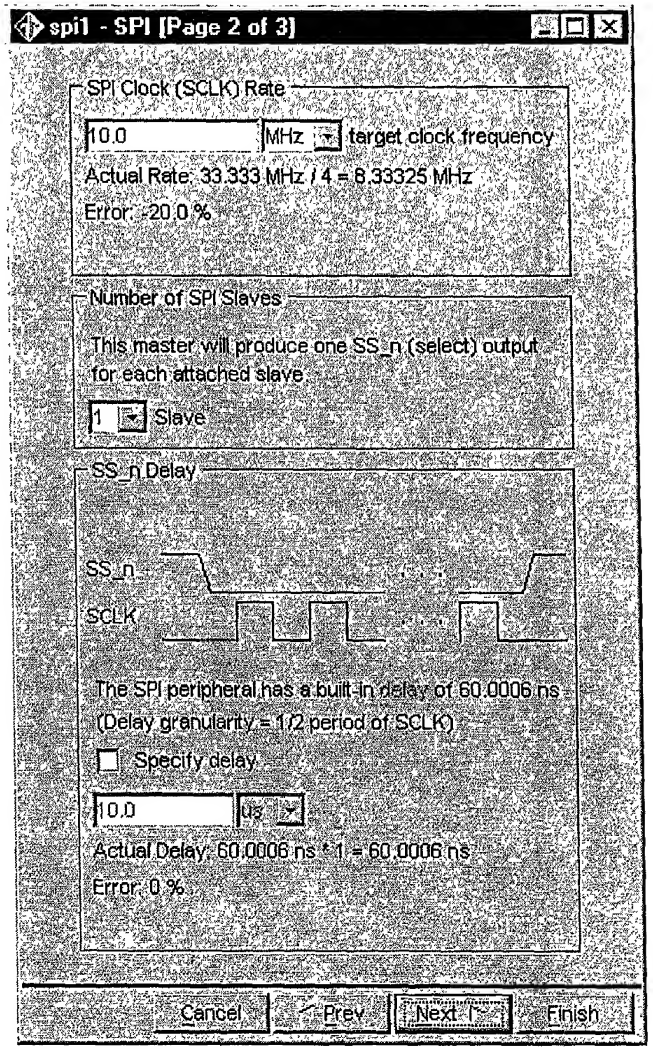


FIGURE 3Q

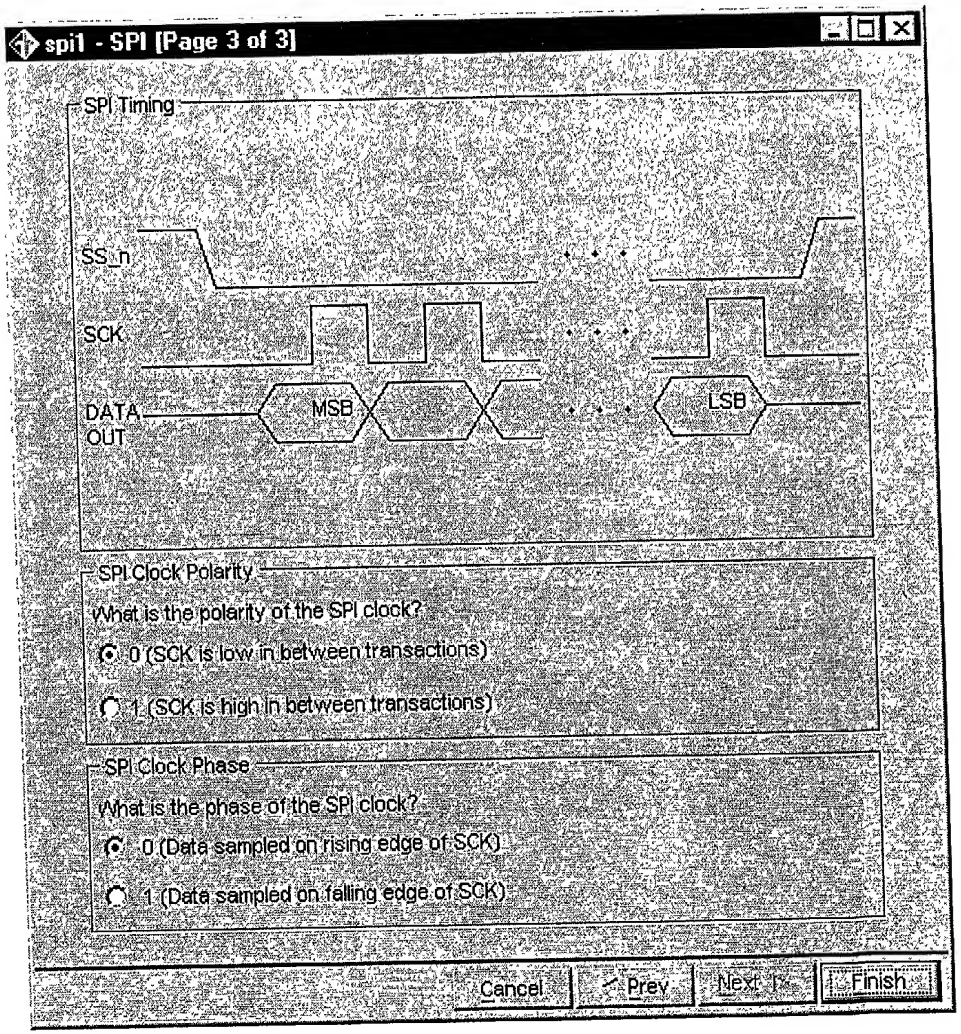


FIGURE 3R

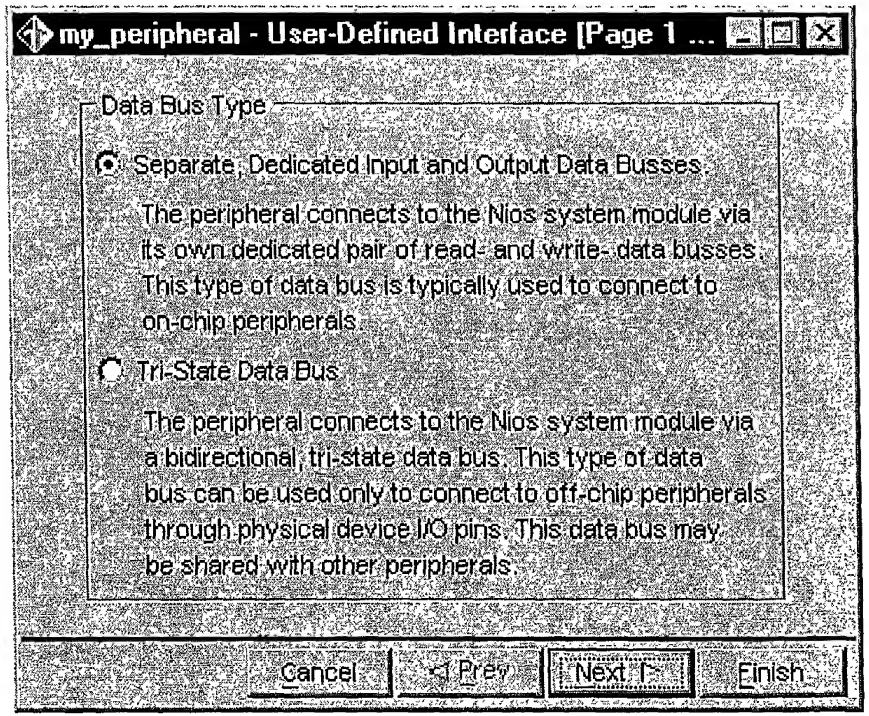


FIGURE 3S

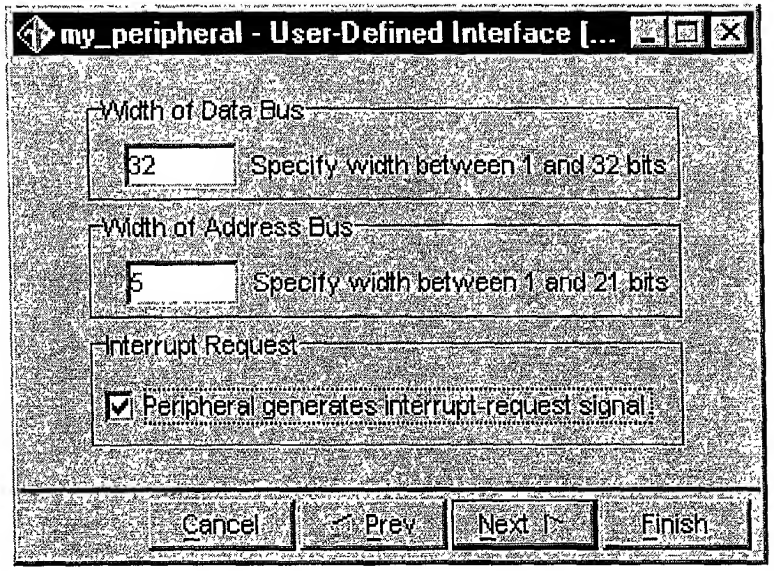


FIGURE 3T

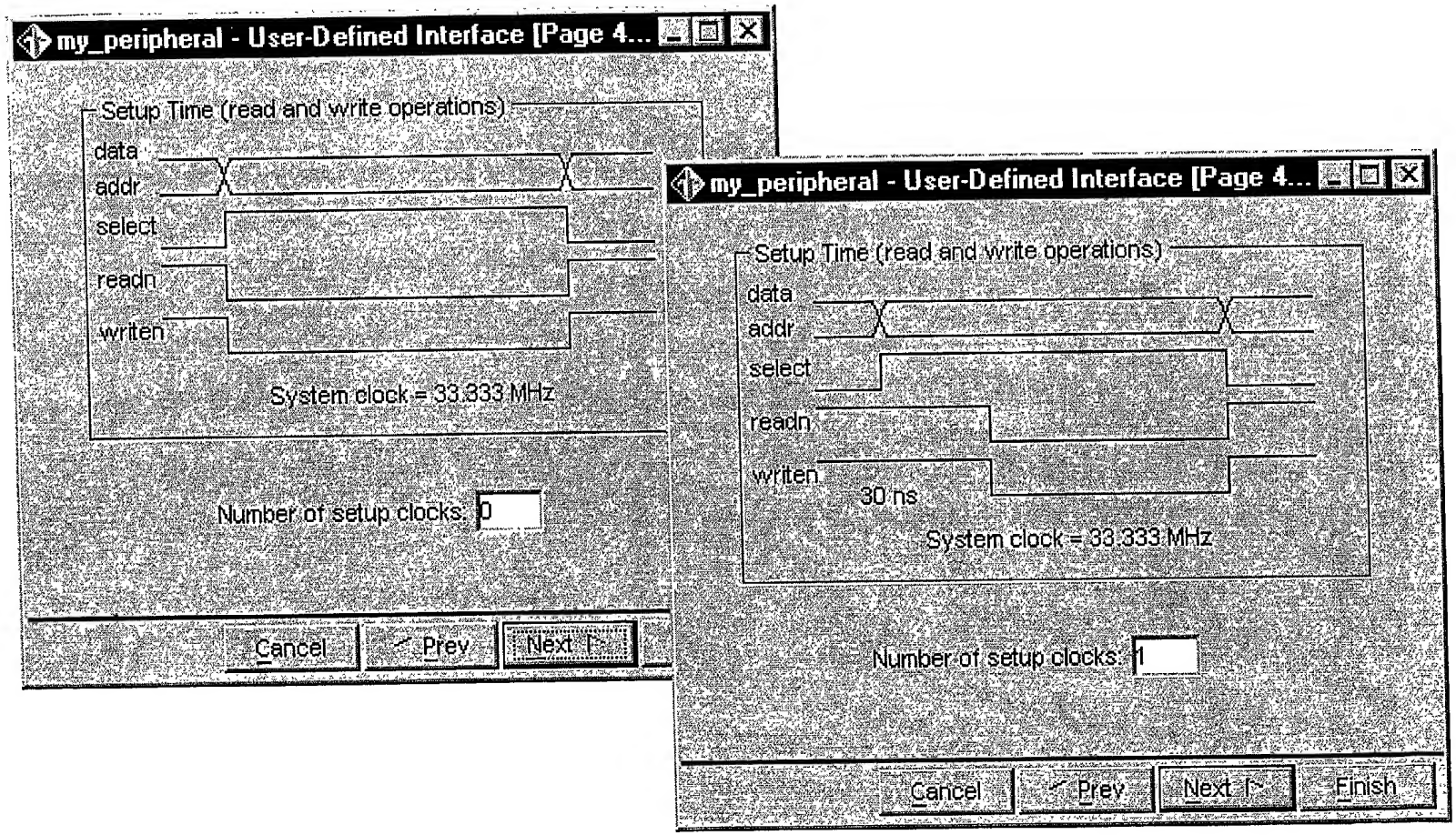


FIGURE 3U

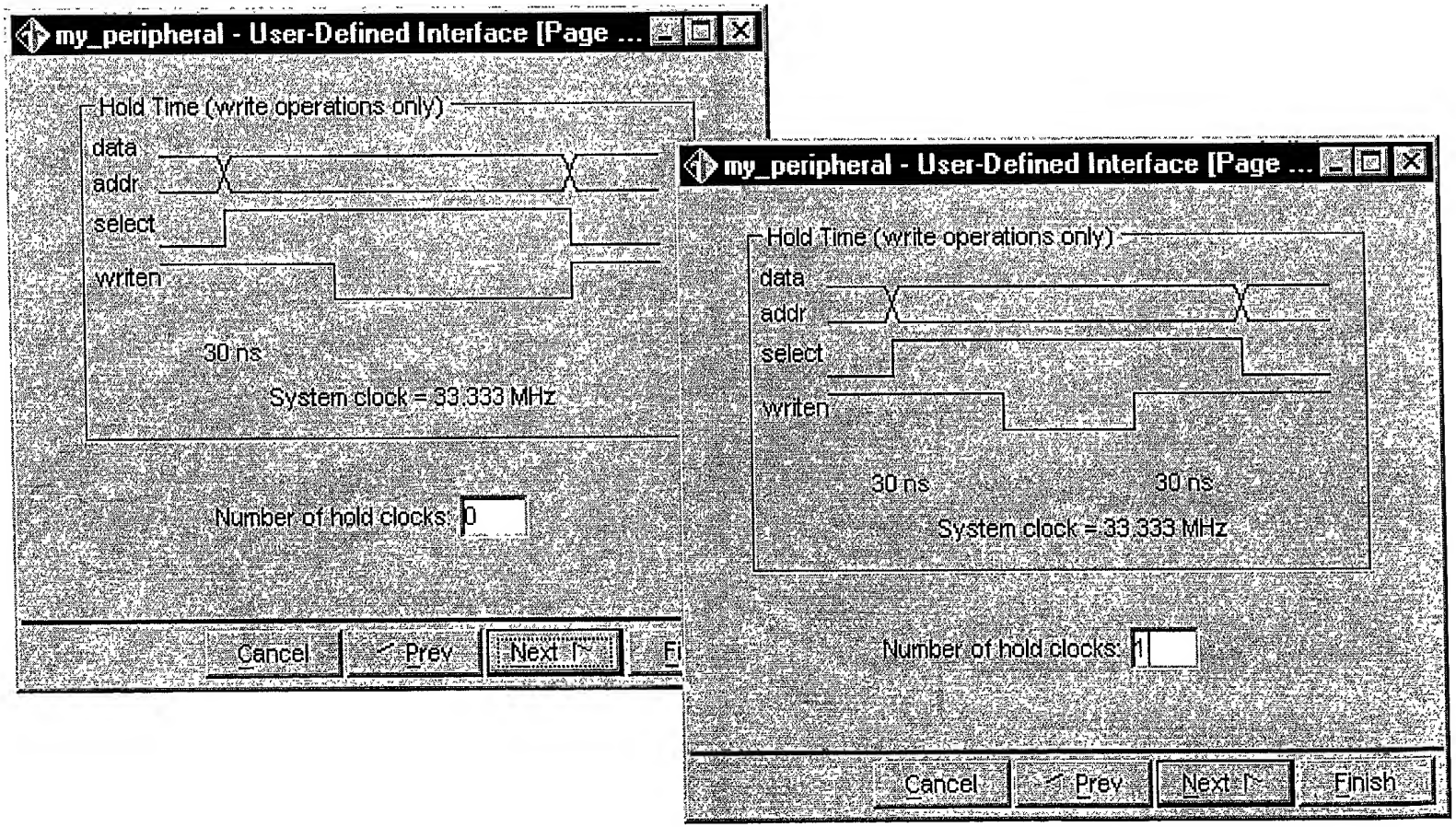

my_peripheral - User-Defined Interface [Page ...
Hold Time (write operations only)
data
addr
select
writen
30 ns
System clock = 33.333 MHz
Number of hold clocks: 0
Cancel
< Prev
Next >
Fi
my_peripheral - User-Defined Interface [Page ...
Hold Time (write operations only)
data
addr
select
writen
30 ns
30 ns
System clock = 33.333 MHz
Number of hold clocks: 1
Cancel
< Prev
Next >
Finish

Figure 3V

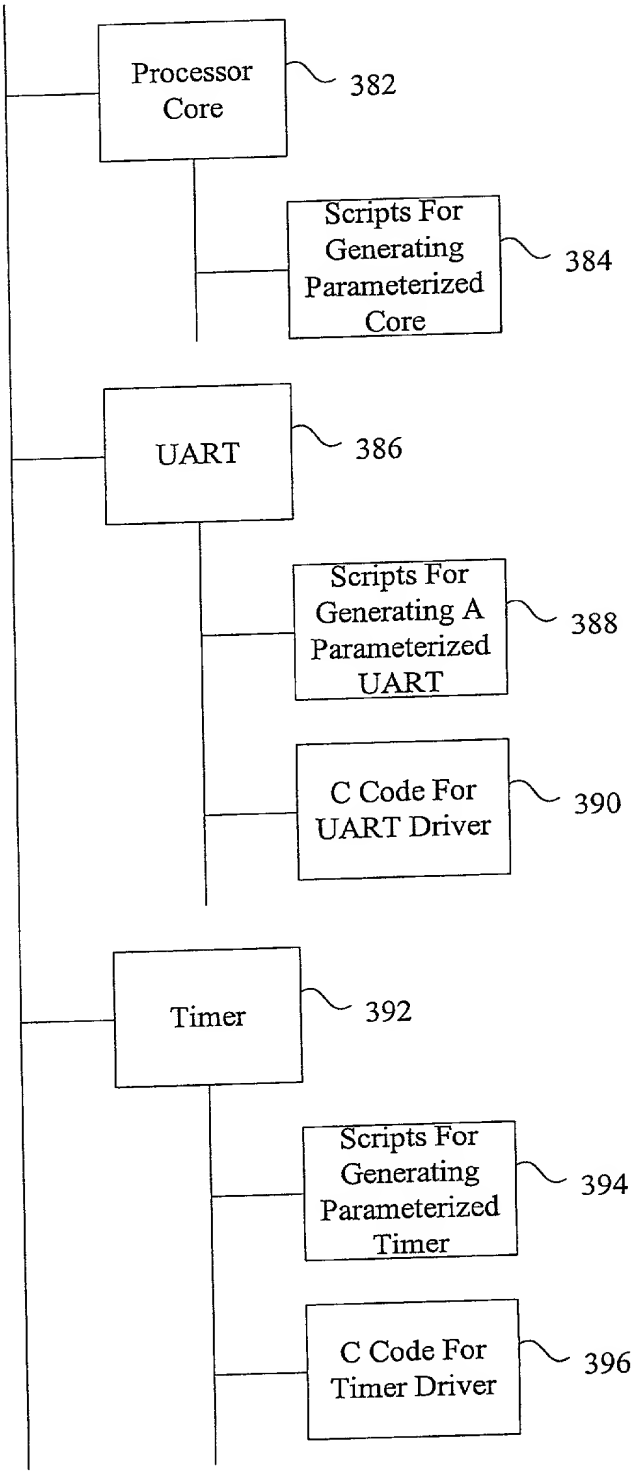

Processor Core
382
Scripts For Generating Parameterized Core
384
UART
386
Scripts For Generating A Parameterized UART
388
C Code For UART Driver
390
Timer
392
Scripts For Generating Parameterized Timer
394
C Code For Timer Driver
396

Figure 4

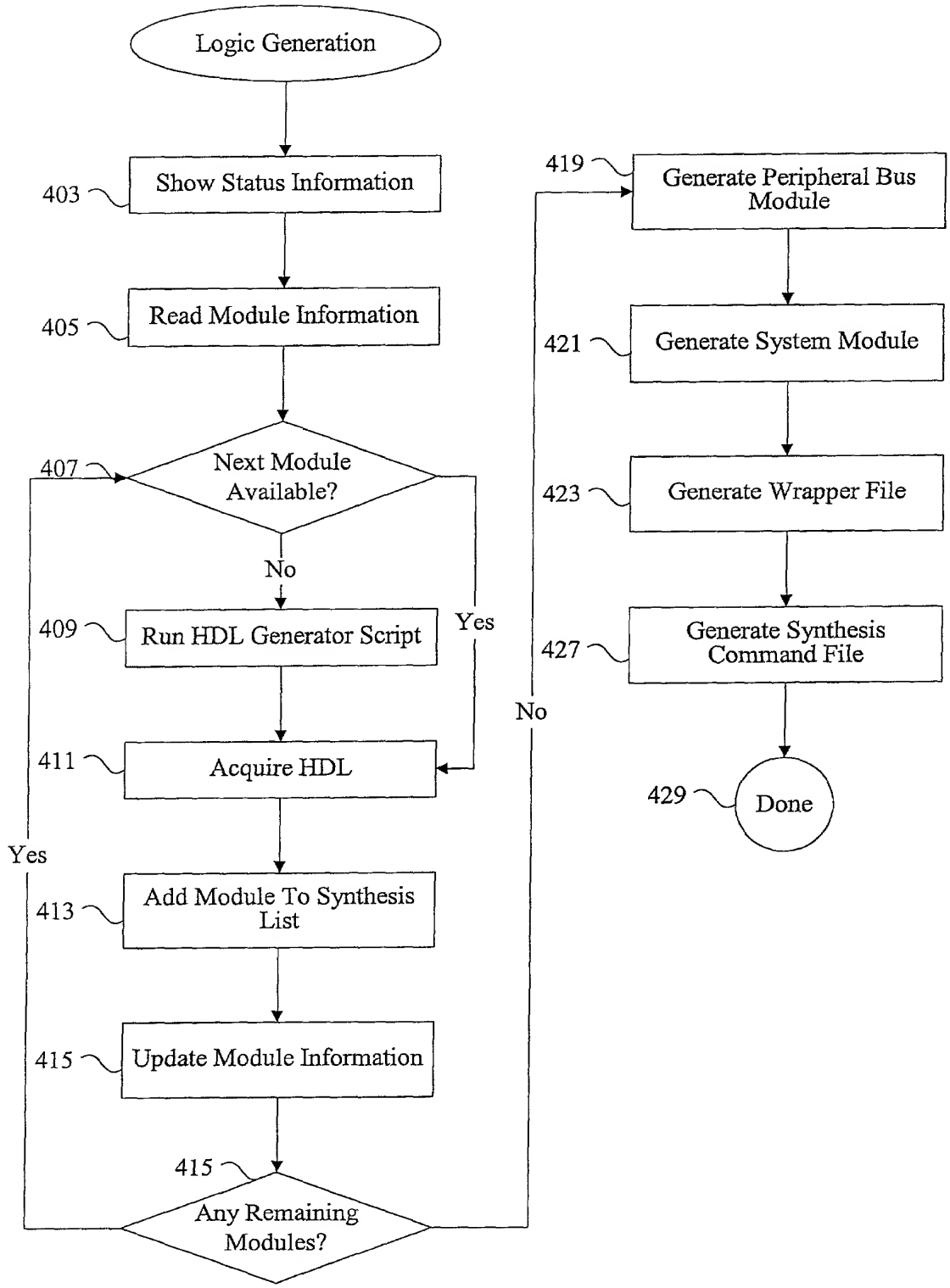

Logic Generation
403
Show Status Information
405
Read Module Information
407
Next Module Available?
No
Yes
409
Run HDL Generator Script
411
Acquire HDL
Yes
413
Add Module To Synthesis List
415
Update Module Information
415
Any Remaining Modules?
No
419
Generate Peripheral Bus Module
421
Generate System Module
423
Generate Wrapper File
427
Generate Synthesis Command File
429
Done

Figure 5

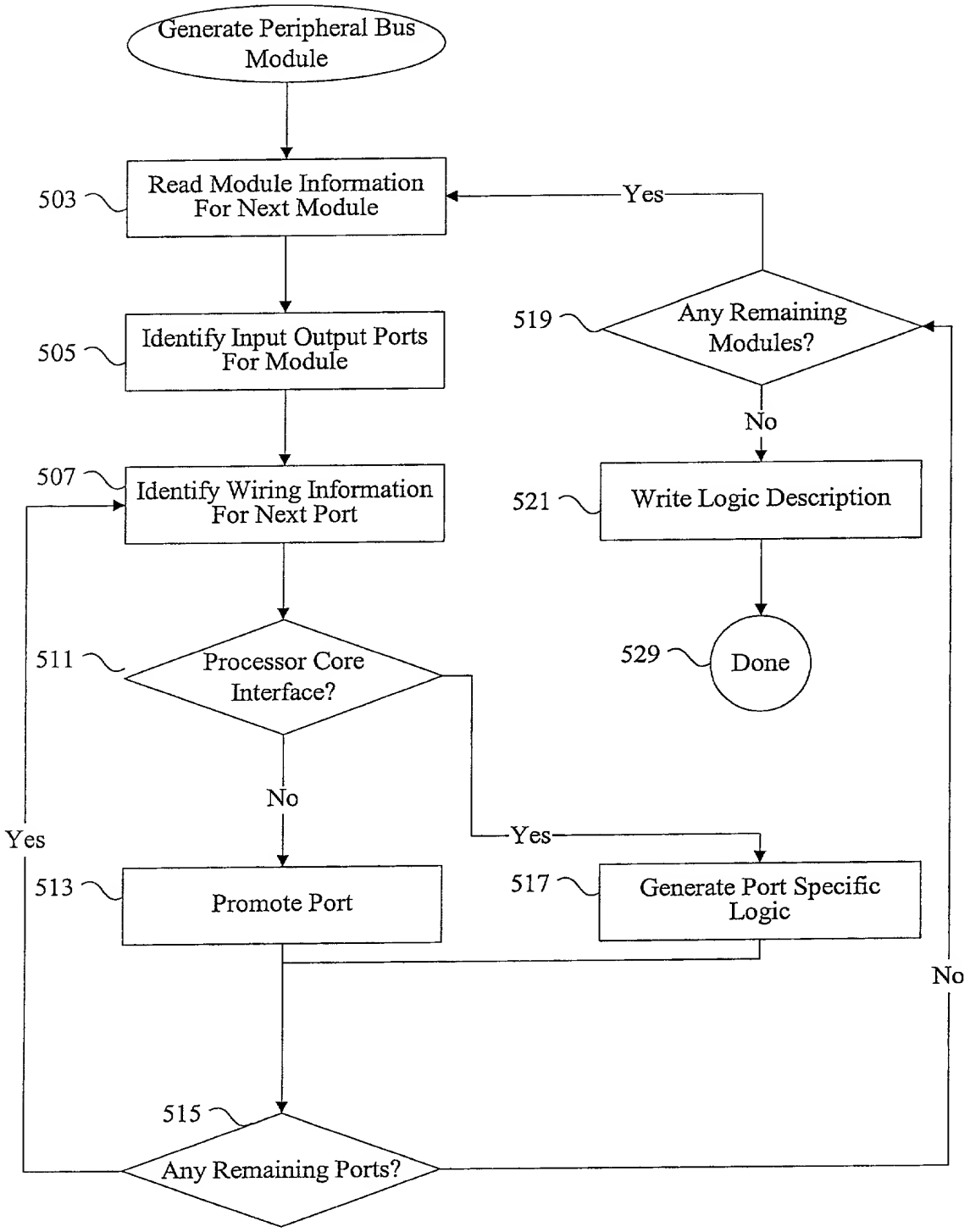

Generate Peripheral Bus Module
503
Read Module Information For Next Module
505
Identify Input Output Ports For Module
507
Identify Wiring Information For Next Port
511
Processor Core Interface?
No
Yes
513
Promote Port
Yes
517
Generate Port Specific Logic
515
Any Remaining Ports?
Yes
519
Any Remaining Modules?
No
521
Write Logic Description
529
Done
No

Figure 6A

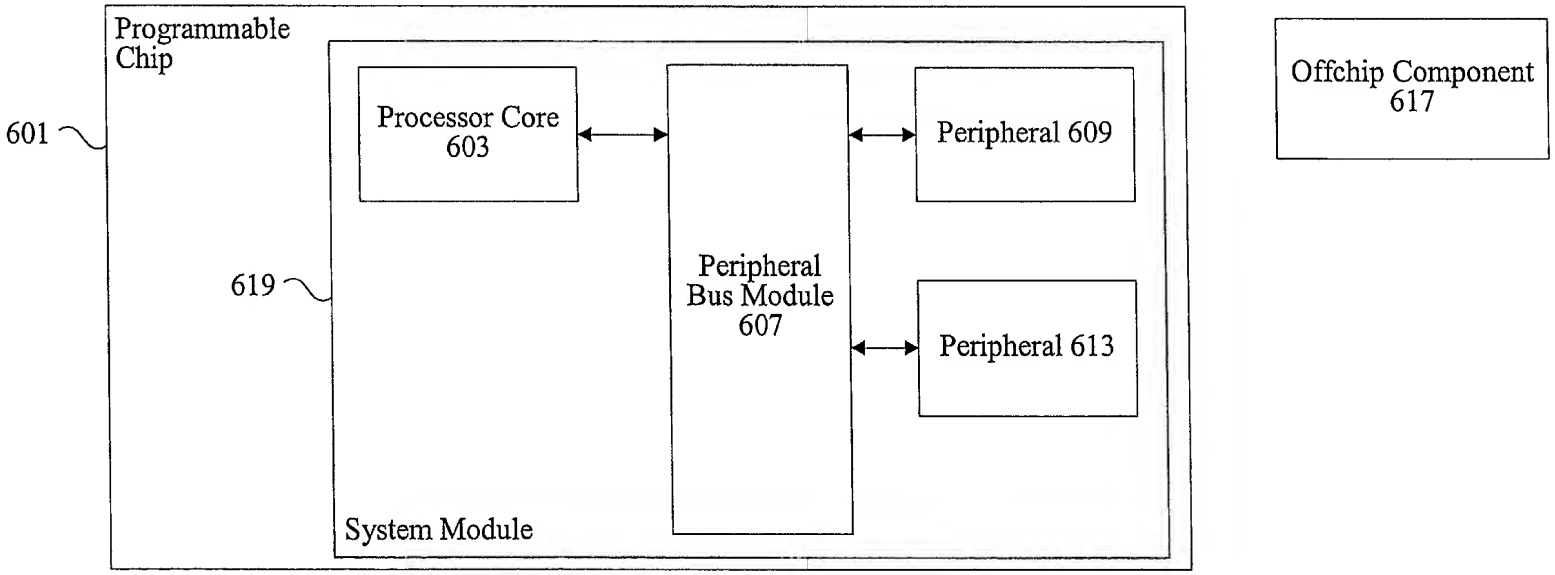

Programmable Chip
601
619
Processor Core 603
Peripheral Bus Module 607
Peripheral 609
Peripheral 613
System Module
Offchip Component 617

Figure 6B

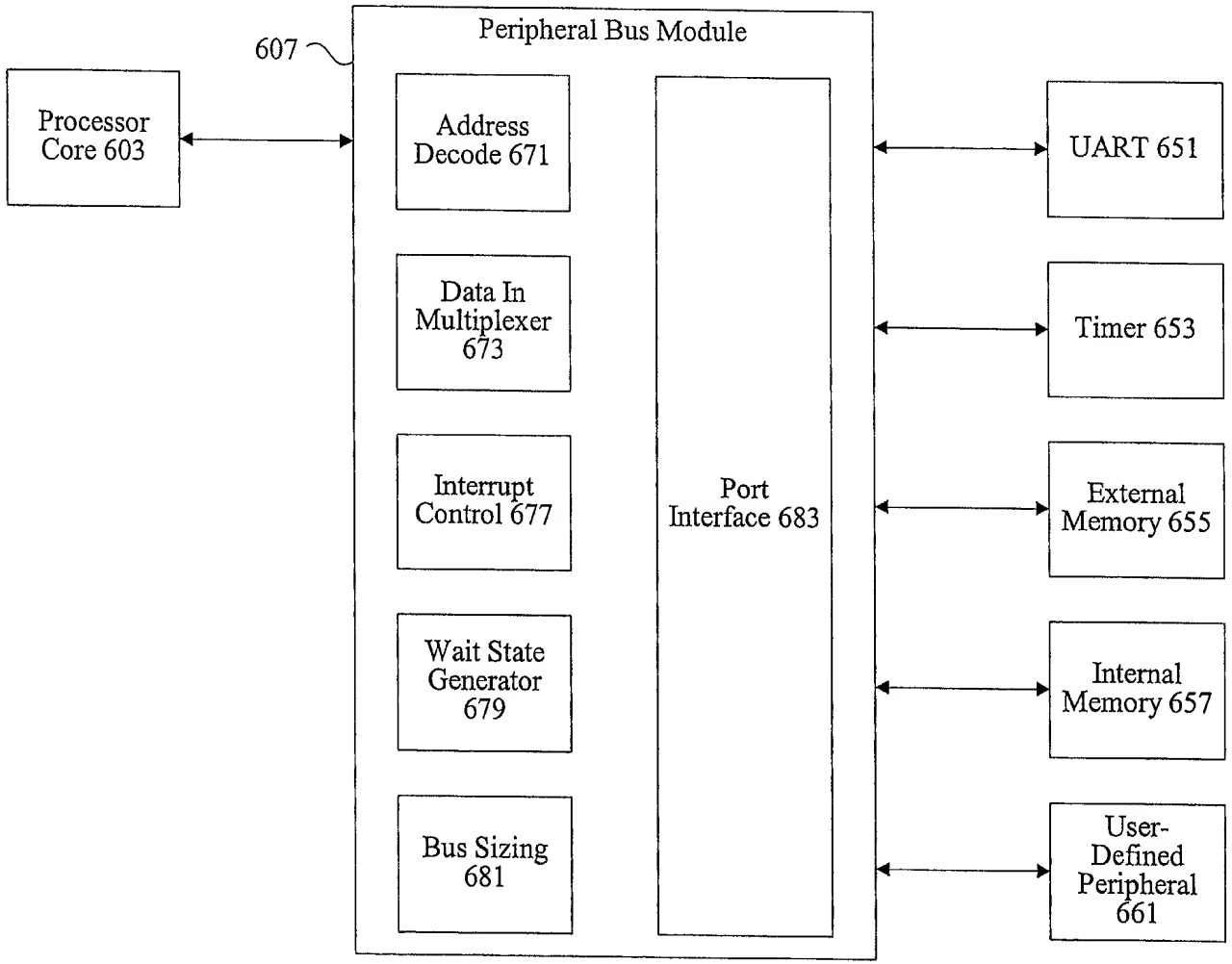


FIGURE 7

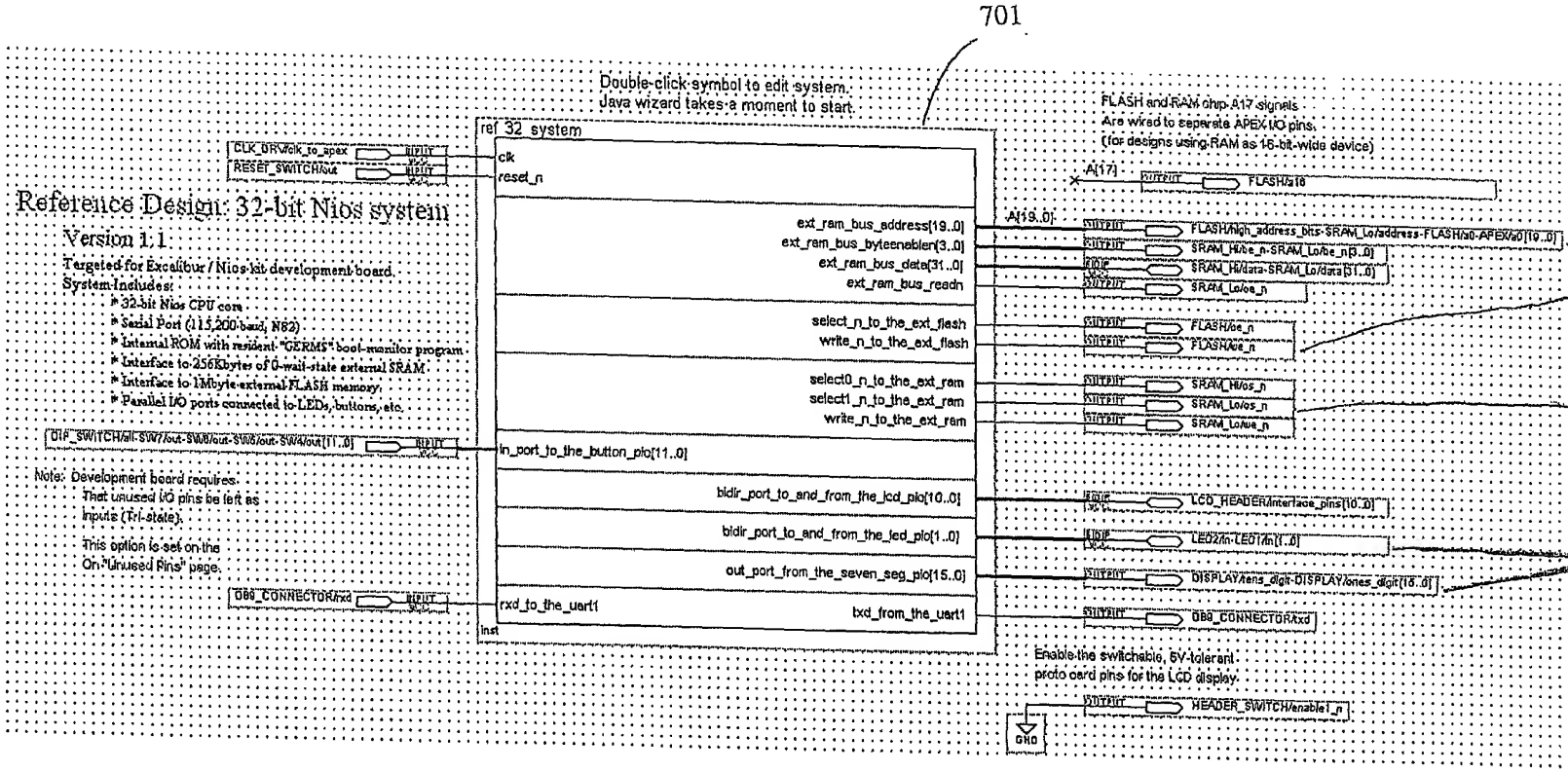
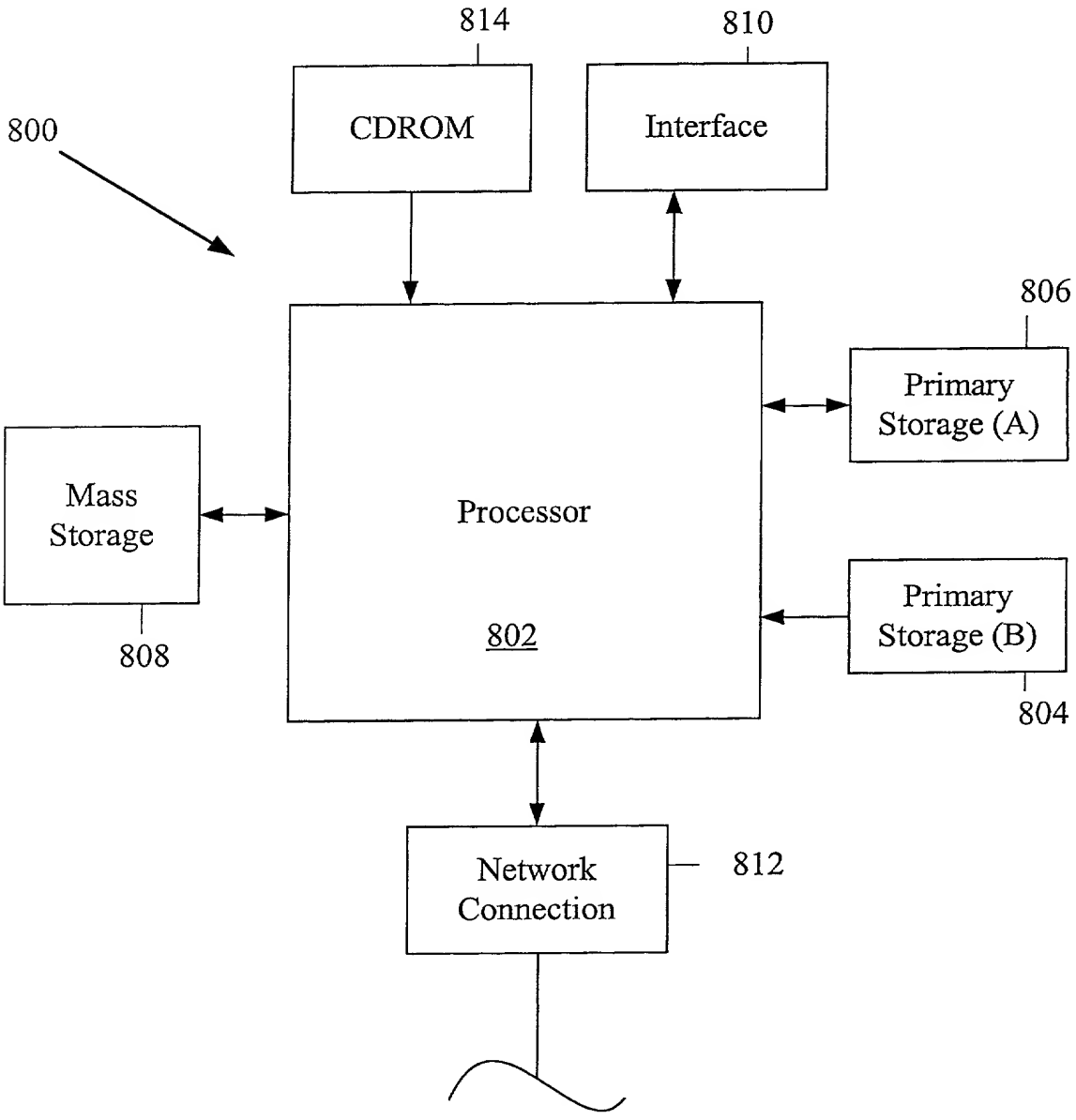


Figure 8


814
810
CDROM
Interface
800
806
Primary Storage (A)
Mass Storage
Processor
802
Primary Storage (B)
808
804
Network Connection
812